

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

TI-35149

Theodore W. Houston

Art Unit: TBD

Serial No: 10/635,185

Examiner: TBD

Filed:

08/06/03

For:

Asymmetric Static Random Access Memory Device Having Reduced Bit Line Leakage

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Karen Vert 11-14-03

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO-1449. A copy of the noted reference is enclosed herewith.

Respectfully submitted,

Rose Alyssa Keagy
Attorney for Applicant

Reg. No. 35,095

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TI-35149

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Sheet

Attorney Docket No.

				U.S. I	PATENT DOCUME	ENTS
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Exam. Initials*	Cite No. ¹	Number	Kind Code ² (if known)	or Applicant of Cited Doc.	of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	CA	NAVID AZIZI ET AL., "Low-Leakage Asymmetric-Cell SRAM" ISLPED '02, August 12-14, 2002, Monterey, California, USA	<u> </u>		
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